

CBCS SCHEME

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21EE32

Third Semester B.E. Degree Examination, June/July 2024 Analog Electronic Circuits and Op-Amps

Time: 3 hrs.

Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

- 1 a. Draw a double ended clipper circuit and explain the working principle with transfer characteristics. (10 Marks)
- b. Derive the expression for stability factor for Voltage Divider Biasing circuit, with respect to I_{CQ} and V_{BE} . (10 Marks)

OR

- 2 a. Define Clamper Circuit. Draw and explain the working of Clamper circuit which clamps the positive peak of a signal to zero. (10 Marks)
- b. The parameters of voltage divider biasing circuit are as $V_{CC} = 16V$, $R_1 = 62 k\Omega$, $R_2 = 9.1 k\Omega$, $R_C = 3.9 k\Omega$, $R_E = 680 \Omega$, $\beta = 80$ and $V_{BE} = 0.7V$. Find the quiescent base current, collector current and V_{CE} . Also determine the values of collector voltage Emitter voltage and base voltage with respect to ground. (10 Marks)

Module-2

- 3 a. Explain the need of cascading amplifier. Draw and explain the block diagram of 2 stage cascade amplifier. (10 Marks)
- b. Explain the concept of feedback with suitable block diagram. (10 Marks)

OR

- 4 a. Draw the circuit of a Darlington emitter follower with voltage divider bias. Calculate input impedance voltage gain and output impedance. Take $\beta_1 = \beta_2 = 100$, $R_1 = R_2 = 100K$, $R_E = 5 k\Omega$. Take $r_e = 0.1 k\Omega$. (10 Marks)
- b. For the current shunt feedback amplifier, derive an expression input resistance and output resistance. (10 Marks)

Module-3

- 5 a. With a neat circuit diagram and waveform, explain the operation of a transforms coupled Class-A power amplifier. Also mention its advantages and disadvantages (Any 3). (10 Marks)
- b. With the help of neat diagram, explain the construction, working and characteristics of P-channel enhancement type MOSFET. (10 Marks)

OR

- 6 a. Explain the operation of Class-B push pull amplifier. Prove that the maximum efficiency of Class-B configuration is 78.5%. (10 Marks)
- b. With a neat circuit diagram, explain the working and characteristics of P-channel JFET. (10 Marks)

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

Module-4

- 7 a. With a neat circuit diagram and frequency response curve, explain the operation of First order lowpass Butterworth filter. Also obtain the expression for gain. (10 Marks)
b. With a neat circuit diagram, explain the working of voltage follower regulator using op-Amp. (10 Marks)

OR

- 8 a. What is an Instrumentation Amplifier? Find the expression for output of 3 op-Amp instrumentation amplifier? (10 Marks)
b. Design a second order low pass filter for a cut-off frequency of 1 kHz and draw its circuit diagram. Assume $C = 1 \mu\text{F}$. (10 Marks)

Module-5

- 9 a. Sketch the circuit of triangular/rectangular waveform generator. Draw the output waveforms from the circuit and explain its operation. (10 Marks)
b. With a neat circuit diagram, explain the working of voltage to current converter with grounded load. Also derive the expression for the same. (10 Marks)

OR

- 10 a. With a neat circuit diagram and waveform explain (i) Integrator (ii) Differentiator. (10 Marks)
b. With a help of neat circuit diagram and waveform explain the working of Inverting Schmitt trigger. Also draw its Transfer characteristics. (10 Marks)
