CBCS SCHEME

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BEC714A

Seventh Semester B.E./B.Tech. Degree Examination, Dec.2025/Jan.2026
Application Specific Integrated Circuits

Time: 3 hrs. Max. Marks: 100

Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.
2. M : Marks , L: Bloom's level , C: Course outcomes.

		Module – 1	M	L	C
Q.1	a.	Bring out the difference between Channelless and Channeled gate array in the ASIC design.	6	L1	CO1
	b.	Calculate the CSD for the binary 011. Assume $C_0 = 0$.	7	L2	CO1
	c.	Show the representation of : i. 1 bit conditional adder ii. Multiplex that selects between sum and carry iii. 4 bit conditional sum adder with carry input.	7	L2	CO1
		OR			
Q.2	a.	Illustrate the ASIC design flow steps with diagram.	7	L2	CO1
	b.	If the change in voltage on a C = 400 pf load by 6V is 8ns, calculate the required current in the output transistors of 3 state bidirectional output buffer.	5	L2	CO1
	c.	Represent : i. Carry save adder cell ii. 4 bit CSA iii. Symbol for a CSA iv. 4 input CSA.	8	L2	CO1
		Module – 2			
Q.3	a.	Define path logical effort, path electrical effort and optimum effort delay.	6	L1	CO3
	b.	Calculate the delay of 3 input NOR logic with 2X drive, driving a net with a fanout of 4 with a total load capacitance comprising the input capacitance of the 4 cells driving plus the interconnect is of 0.5pf. Assume $p_{inv} = 1.5$, $q_{inv} = 2.0$ and $C_{inv} = 0.08$pf.	8	L3	CO3
	c.	Show the ACTEL Act 2 and Act 3 logic modules.	6	L1	CO3

OR

Q.4	**a.**	Calculate setup time, hold time and clock to output delay in case of S-module of ACTEL Act 2 model. Assume t'_{sud} = 0.8ns, t'_H = 0.2ns, t'_{co} = 0.5ns, t'_{pd} = 5ns, t'_{clkD} = 3ns.	6	L3	CO2
	b.	Calculate the approximate total logical area for the circuit shown in Fig.Q4(b).	6	L3	CO2

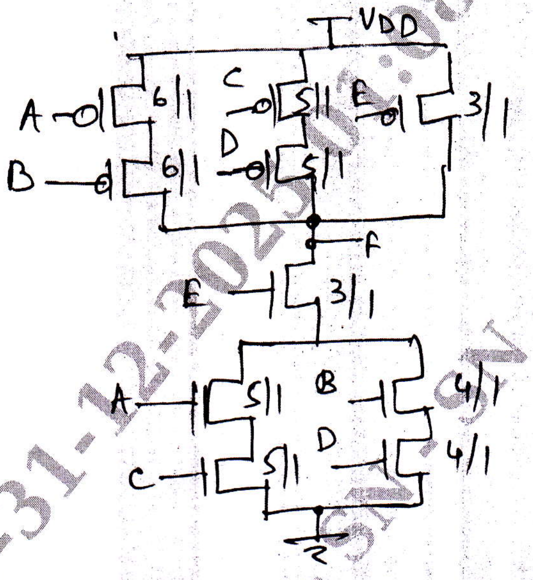


Fig.Q4(b)

	c.	Write the Xilinx XC3000 CLB and list the important features.	8	L1	CO3

Module – 3

Q.5	**a.**	Explain on cell library, schematic icons and nets in the schematic entry of the ASIC design.	10	L2	CO5
	b.	Estimate the ASIC die size of a 50K gate ASIC in a 0.35 μm gate a array 3 level metal process with 166 I/O pads. Assume standard cell density is 5×10^{-4} gate/λ^2, gate array utilization is 0.6 to 0.8 and routing factor is 1 to 2.	10	L4	CO5

OR

Q.6	**a.**	State the goals and objectives of the ASIC physical design steps.	10	L3	CO5
	b.	For the network shown in Fig.Q6(b), write the network graph. Define net cutset and edge cutset. Calculate the corresponding edge cutset for the net cutset shown in figure.	10	L3	CO5

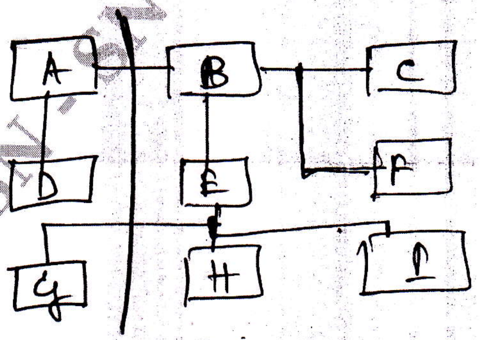
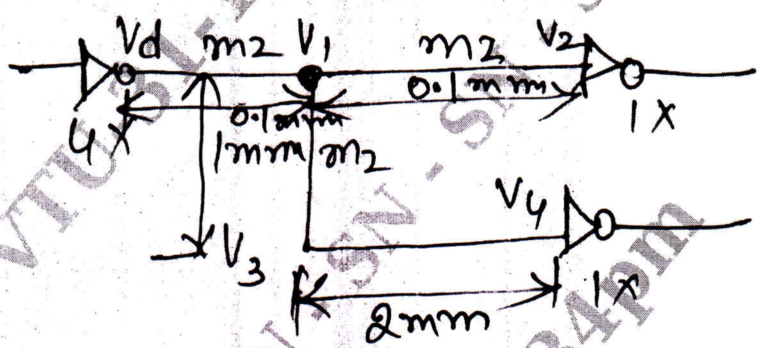


Fig.Q6(b)

Module – 4					
Q.7	**a.**	Show the channel routing order for a slicing floor path using a slicing free and non-slicing floor plan with a cyclic constrain.	**10**	**L2**	**CO5**
	b.	Explain zero stack algorithm with no net delay.	**10**	**L2**	**CO4**
OR					
Q.8	**a.**	Show the pad limited die and core limited die with diagram.	**10**	**L2**	**CO4**
	b.	Explain pair wise interchange and force directed placement.	**10**	**L2**	**CO4**
Module – 5					
Q.9	**a.**	Calculate the delay of a net at node 4 shown in Fig.Q9(a). Assume m^2 resistances s 50 mΩ/square, m^2 capacitance is 0.2 pf/mm, m^2 minimum width is 0.9/µm.  Fig.Q9(a)	**10**	**L4**	**CO4**
	b.	Explain clock routing in special routing method.	**10**	**L2**	**CO4**
OR					
Q.10	**a.**	Illustrate finding paths method in global routing in a cell based ASIC.	**10**	**L2**	**CO4**
	b.	Illustrate left edge algorithm used in routing.	**10**	**L2**	**CO4**

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