CBCS SCHEME - Make-Up Exam

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BEC302

Third Semester B.E./B.Tech. Degree Examination, June/July 2025
Digital System Design using Verilog

Time: 3 hrs. Max. Marks: 100

Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.
2. M : Marks , L: Bloom's level , C: Course outcomes.

		Module – 1	M	L	C
Q.1	a.	Define combinational logic circuit. Explain design procedure of combinational circuit.	6	L1	CO1
	b.	Covert $x = \bar{a}b + bc$ to canonical form.	4	L1	CO1
	c.	Find all prime implicants of using Quin-McClusky method and simplify it $Z = f(a,b,c,d) = \Sigma m(1,2,3,5,9,12,14,15) + \Sigma d(4,8,11)$.	10	L1	CO1
		OR			
Q.2	a.	Define literals and solve the following equation using canonical form : i) $P = f(a,b,c) = a\bar{b} + a\bar{c} + bc$ ii) $Q = f(a,b,c) = (a + \bar{b})(\bar{b} + c)$ iii) $R = f(a,b,c) = A + ABC$.	10	L1	CO1
	b.	Simplify the following expression using K-map. Implement the simplified expression using basic gates only. i) $F(a,b,c,d) = \Sigma m(1,3,7,11,15) + \Sigma d(0,2,4)$ ii) $F(a,b,c,d) = \pi M(0,4,8,12,13,14,15)$.	10	L1	CO1
		Module – 2			
Q.3	a.	Draw the block diagram of 4-bit look ahead carry adder. Derive the expressions for the carry outputs using propagate and generate inputs.	10	L2	CO2
	b.	Implement full adder and full subtractor using 74138 decoder.	10	L2	CO2
		OR			
Q.4	a.	Design 2-bit comparator using gates.	10	L3	CO2
	b.	Implement following two outputs function using 74LS138 and external gates : $F_1(A,B,C) = \Sigma m(1,4,5,7)$ $F_2(A,B,C) = \pi m(2,3,6,7)$.	5	L3	CO2
	c.	Implement following Boolean function using 8 : 1 MUX. $F(P,Q,R,S) = \Sigma m(0,1,3,4,8,9,15)$.	5	L3	CO2

		Module – 3			
Q.5	**a.**	Define sequential circuit. Explain the operation of a switch debouncer using S-R Latch with help of circuits and waveform.	**10**	**L1**	**CO3**
	b.	Explain the working of master-slave JK flip-flop with functional table and timing diagram.	**10**	**L2**	**CO3**
		OR			
Q.6	**a.**	Find characteristics equation for SR, JK, D and T flip-flop with the help of function table.	**10**	**L1**	**CO3**
	b.	Construct mod – 6 synchronous counter using JK flip-flop.	**10**	**L4**	**CO3**
		Module – 4			
Q.7	**a.**	Define HDL. List all data types in verilog HDL. Explain any two data types.	**10**	**L1**	**CO4**
	b.	Explain the various types of logical operators with an example.	**10**	**L2**	**CO4**
		OR			
Q.8	**a.**	Explain classification of types of description with an example.	**10**	**L2**	**CO4**
	b.	i) Write verilog code for full adder ii) Write verilog code for 8 : 1 MUX.	**10**	**L1**	**CO4**
		Module – 5			
Q.9	**a.**	Write a verilogy structure code for four bit ripple carry adder.	**10**	**L1**	**CO4**
	b.	Explain structure of behavioural description with example.	**10**	**L2**	**CO4**
		OR			
Q.10	**a.**	Write a verilog behavioural code for 4 to 1 MUX using case statement.	**10**	**L1**	**CO4**
	b.	Explain with block diagram the components of a verilogy module by highlighting mandatory blocks.	**10**	**L2**	**CO4**

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