

CBCS SCHEME

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BCS302

Third Semester B.E/B.Tech. Degree Examination, Dec.2025/Jan.2026

Digital Design and Computer Organization

Time: 3 hrs.

Max. Marks:100

Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.

2. M : Marks , L: Bloom's level , C: Course outcomes.

Module – 1			M	L	C
1	a.	Obtain the minimum expression for the POS expression : $F(A, B, C, D) = \pi M(0, 1, 5, 7, 9, 13, 15) + d(3, 10).$	5	L2	CO1
	b.	Implement the following logic function in SOP form using NOR gates. $Y = A\bar{B} + B\bar{C} + ABC.$	5	L3	CO1
	c.	Identify the essential prime implicants of the following functions : $F(w, x, y, z) = (0, 1, 4, 5, 6, 7, 9, 11, 14, 15)$ $F(A, B, C, D) = (0, 2, 3, 5, 7, 8, 10, 11, 14, 15).$	10	L3	CO1
OR					
2	a.	Demonstrate the positive and negative logic using AND gate.	5	L2	CO1
	b.	Simplify the following Boolean functions using K-map : i) $F(P, Q, R, S) = \Sigma(0, 2, 5, 7, 8, 10, 13) + d(1, 4, 15)$ ii) $F(A, B, C, D) = (\bar{A} + B + C)(\bar{A} + \bar{C} + D)(\bar{B} + C + D).$	10	L3	CO1
	c.	Explain Dataflow Modeling in verilog with an example program.	5	L1	CO1
Module – 2					
3	a.	Explain the difference between combinational and sequential circuits with their block diagrams and examples.	5	L2	CO2
	b.	Write the verilog program to implement full adder and full subtractor circuits.	7	L2	CO2
	c.	Describe and explain 4 bit adder with carry look ahead.	8	L3	CO2
OR					
4	a.	Implement the Boolean function : $F(A, B, C, D) = \Sigma m(1, 3, 4, 11, 12, 13, 14, 15)$ using 8 : 1 MUX.	5	L3	CO2
	b.	What is encoder? Design 8 : 3 encoder circuits with logic diagram and truth table and also list its applications.	7	L3	CO2
	c.	What is Latch? Demonstrate the working of SR flip-flop and D Flip-flop and write the characteristics table and equations.	8	L3	CO2
1 of 2					

Module – 3

5	a.	What do you mean by an addressing mode? Explain any 5 addressing modes.	10	L2	CO3
	b.	Describe the Big-endian and Little-endian address assignment.	5	L1	CO3
	c.	A program with 5000 machine instructions needs an average of 3 basic steps to execute one instruction. Find the performance of the computer having a clock speed of 500 KHz.	5	L3	CO3

OR

6	a.	Demonstrate the Branching operations using loop to add n numbers with block diagram.	8	L3	CO3
	b.	Show how below expression will be executed in one address and three address processor in accumulator organization. $X = (A * B) + (C * D)$.	7	L3	CO3
	c.	What are Condition Code Flags? Mention the significance of the flag N, Z, V and C.	5	L1	CO3

Module – 4

7	a.	Explain memory mapped I/O and I/O interface for an input device with a diagram.	10	L2	CO4
	b.	Explain DMA with a neat diagram.	10	L4	CO4

OR

8	a.	Explain how to handle interrupt from multiple devices using daisy chain and priority scheme.	10	L3	CO4
	b.	Explain centralized and distributed Bus Arbitration approaches.	10	L2	CO4

Module – 5

9	a.	With a diagram, explain the single bus organization of the data path inside a processor.	10	L2	CO5
	b.	Describe the basic idea of instruction pipeline.	10	L2	CO5

OR

10	a.	Explain the process of fetching word from memory in processor.	10	L4	CO5
	b.	Explain the pipeline performance of a processor and pipeline stalls.	10	L2	CO5
