USN | | | | | | | | | | |

08EC029

M.Tech. Degree Examination, Dec.09/Jan.10
Digital Circuits & Logic Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions.***

1 a. Explain the concept of threshold logic. **(05 Marks)**

b. Determine the function $f(x_1, x_2, x_3, x_4)$ realized by the network shown in Fig.1(b). **(06 Marks)**

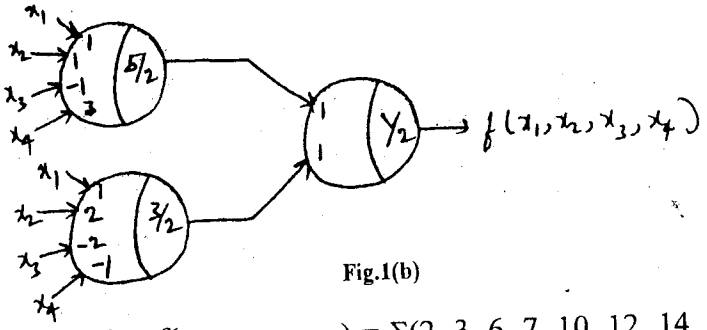

Fig.1(b)

c. Given the switching function $f(x_1, x_2, x_3, x_4) = \Sigma(2, 3, 6, 7, 10, 12, 14, 15)$. Find a minimal threshold logic realization. **(09 Marks)**

2 a. For the circuit shown in Fig.2(a), wires m, n, p & q may become either s-a-0 or s-a-1. Determine a minimal fault-detection experiment by means of fault table. **(10 Marks)**

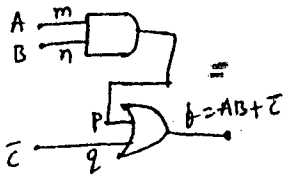

Fig.2(a)

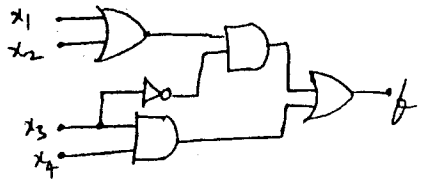

Fig.3(a)

b. What are critical and sub-critical errors? Determine the same for AND, OR, NAND, NOR & EX-OR gates. **(05 Marks)**

c. With a net diagram, explain the basic structure of a quadded network. **(05 Marks)**

3 a. For the circuit shown in Fig.3(a), find all tests to detect the faults x_3, s-a-0 & x_3 s-a-1. **(10 Marks)**

b. Use the map method to find a minimal set of tests for multiple faults for the two-level AND-OR realization of the function **(10 Marks)**

$$f(w, x, y, z) = w\bar{z} + x\bar{y} + \bar{w}x + w\bar{x}y$$

4 a. For the m/c shown in Table 4(a), find the equivalence partition and a corresponding reduced m/c in standard form. **(10 Marks)**

P.S.	NS, Z	
	x = 0	x = 1
A	F, 0	B, 1
B	G, 0	A, 1
C	B, 0	C, 1
D	C, 0	B, 1
E	D, 0	A, 1
F	E, 1	F, 1
G	E, 1	G, 1

Table 4(a)

b. Draw the merger graph and compatibility graph and determine the minimal closed covering for the m/c shown in Table 4(b). (10 Marks)

Table 4(b)

P.S.	NS, Z			
	I_1	I_2	I_3	I_4
A	-	-	E, 1	-
B	C, 0	A, 1	B, 0	-
C	C, 0	D, 1	-	A, 0
D	-	E, 1	B, -	-
E	B, 0	-	C, -	B, 0

5 a. The m/c shown in Table 5(a) has the following closed partitions. $\pi_1 = \{\overline{ACE}; \overline{BDF}\}$, $\pi_2 = \{\overline{AF}; \overline{BE}; \overline{CD}\}$.

i) Find a state assignment which reduces the interdependencies of the state variables.

ii) Derive the logical equations and show the circuit diagram when unit delays are used as memory elements. (10 Marks)

Table 5(a)

P.S.	NS		Z
	x = 0	x = 1	
A	D	C	1
B	A	D	0
C	B	E	0
D	E	B	0
E	F	C	0
F	C	D	0

b. For the m/c shown in Table 5(b) find the π - lattice. (10 Marks)

Table 5(b)

P.S.	NS	
	x = 0	x = 1
A	D, 0	C, 0
B	C, 0	D, 1
C	E, 0	F, 0
D	F, 0	F, 1
E	G, 0	H, 0
F	H, 0	G, 1
G	B, 0	A, 0
H	A, 0	B, 1

6 a.

Table 6(a)

P.S.	NS		Z	
	x = 0	x = 1	x = 0	x = 1
A	D	B	0	0
B	A	C	1	0
C	B	E	1	0
D	F	A	0	1
E	F	C	0	0
F	E	D	0	1

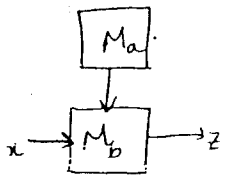

Fig.6(a)

i) Determine state assignment for the m/c shown in Table 6(a) so that it will have the structure shown in Fig.6(a).

ii) Show the state diagram of the input-independent component. (10 Marks)

b.

P.S	x_1x_2	NS		Z
	00	01	10	
A	C	B	D	0
B	A	E	C	0
C	E	B	D	0
D	C	C	E	0
E	E	D	B	1

Table 6(b)

Determine the set of all Mm pairs for the machine shown in Table 6(b) (10 Marks)

7 a. For the m/c shown in Table 7(a), determine the synchronizing tree and synchronizing sequence to synchronize the m/c to state D. **(10 Marks)**

Table 7(a)

P.S.	NS, Z	
	x = 0	x = 1
A	B, 0	D, 0
B	A, 0	B, 0
C	D, 1	A, 0
D	D, 1	C, 0

b. For the m/c shown in Table 7(b) construct the distinguishing tree. Obtain all possible distinguishing sequences. Write the response of m/c to the sequence 111. **(10 Marks)**

Table 7(b)

P.S.	NS, Z	
	x = 0	x = 1
A	C, 0	D, 1
B	C, 0	A, 1
C	A, 1	B, 0
D	B, 0	C, 1

8 a. Identify the m/c which is known to have two states and its response to the i/p sequence X is the o/p sequence Z, as shown below:

Time :	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8
X :	1	1	1	0	1	0	1	
Z :	0	1	0	0	1	0	0	

(10 Marks)

b. What is a diagnosable sequential m/c? Construct testing table and graph for the m/c shown in Table 8(b). **(10 Marks)**

Table 8(b)

P.S.	NS, Z	
	x = 0	x = 1
A	B, 0	D, 0
B	A, 0	B, 0
C	D, 1	A, 0
D	D, 1	C, 0

* * * * *