M.Tech. Degree Examination, Dec.09/Jan.10

CMOS VLSI Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions.***

1 a. With neat sketches, explain the behaviour of nMOS device under the influence of different terminal voltages (Enhancement mode). **(09 Marks)**

b. Explain small signal model for an MOS transistor. **(06 Marks)**

c. Write a note on differential inverter. **(05 Marks)**

2 a. Explain λ based design rules. **(08 Marks)**

b. Obtain the scaling factors for the following:

i) Gate capacitance C_g

ii) Saturation current I_{dss}

iii) Parasitic capacitance. **(06 Marks)**

c. Define sheet resistance and also explain the concept applied to MOS transistor and inverters. **(06 Marks)**

3 a. Explain the second order effects associated with a MOSFET. **(10 Marks)**

b. Explain twin tub CMOS process. **(10 Marks)**

4 a. Explain the effect of long polysilicon wires. Show how to improve the signal propagation. **(04 Marks)**

b. Derive the threshold voltage equation (V_t) for 2 inputs CMOS NOR gate ($V_{t\,NOR2}$). **(10 Marks)**

c. For the given function $f = \overline{A}B + A\overline{C} + A(B + D)$, obtain

i) CMOS TG realization

ii) CMOS transistor realisation **(06 Marks)**

5 a. Explain the function of D latch with gate level schematic and CMOS circuit. **(06 Marks)**

b. Explain synchronous dynamic circuit implemented using depletion load nMOS. **(09 Marks)**

c. Explain the principle of pass transistor circuit. **(05 Marks)**

6 a. Discuss the general principle of band gap reference and hence obtain expression for V_{BE}. **(08 Marks)**

b. Explain cross operational amplifier with necessary expression and characteristics. **(08 Marks)**

c. Mention the advantages of CMOS over NMOS. **(04 Marks)**

7 a. Describe different clock distribution schemes. **(06 Marks)**

b. Mention the causes of latch up and guidelines for avoiding latch up. **(10 Marks)**

c. Realize the following function Z = AB + (C + D) (E + F) + GH using

i) Standard CMOS

ii) Domino CMOS. **(04 Marks)**

8 Write short notes on:

a. BICMOS circuit

b. Dynamic CMOS logic

c. Voltage boot strapping

d. Current mirror. **(20 Marks)**

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