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08EC021

M.Tech. Degree Examination, Dec.08/Jan.09
CMOS VLSI Design

Time: 3 hrs. Max. Marks:100

Note: 1. ***Answer any FIVE full questions.***
2. ***Assume missing data if any, suitably.***

1 a. How does the nmos-enhancement mode transistor function, in different regions of operation? Explain with neat sketches and output characteristics. (08 Marks)
b. What are the second order effects in a MOSFET? Explain. (12 Marks)

2 a. With neat fabrication sketches, explain the fabrication of a cmos inverter. (12 Marks)
b. Obtain the scaling factors for the following gate capacitance C_g, gate delay T_d, Maximum operating frequency f_0 and current density J. (08 Marks)

3 a. Define sheet resistance, standard unit of capacitance and delay unit J. (06 Marks)
b. Derive the expressions for rise time and fall time of a cmos inverter. (08 Marks)
c. A mos layer in 5 μm wide, 60 μm long and 1 μm thick. The resistivity of the layer is 1 Ωcm. Using the sheet resistance concept, calculate the resistance of the mos layer along its length. (06 Marks)

4 a. Provide the λ-based design rules for double metal, cmos process technology, for all layers, transistors and contacts. (10 Marks)
b. Draw the cmos circuit and stick diagram for the function $\overline{(AB+C)D}$. (06 Marks)
c. What are the disadvantages of nmos and pmos pass transistors? How is the transmission gate useful in this regard? (04 Marks)

5 a. With a neat circuit diagram, showing the parasitic capcitance, explain cmos 2 input NOR gate and specify the condition for Kn and Kp to get $Vth = \frac{VDD}{2}$. (08 Marks)
b. Realize the functions,
i) $A = xy + x'y' + xy'z$ and
ii) $B = x'y + xy'$
using transmission gates. (06 Marks)
c. Draw the cmos logic circuit for the function $\overline{(D+E+A)(B+C)} = Z$. (06 Marks)

6 a. Explain the function of a SR latch using NAND2 gates with gate level schematic and cmos circuit. (06 Marks)
b. What is voltage boot strapping? Explain. (08 Marks)
c. Explain the phenomenon of charge storage and charge leakage in a nmos pass transistor. (06 Marks)

7 a. Explain the operation of a cmos differential amplifier with neat circuit. (08 Marks)
b. Describe the different clock distribution schemes. (06 Marks)
c. With neat circuit diagram explain NORA CMOS logic (NP – Domino logic). (06 Marks)

8 Write short notes on:
a. Domino cmos logic.
b. Bicmos circuits.
c. Cmos process enhancement.
d. S.O.I technology. (20 Marks)

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