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12EC003

**M.Tech. Degree Examination, June / July 2014**  
**Advanced Computer Architecture**

Time: 3 hrs.

Max. Marks:100

**Note: Answer any FIVE full questions.**

- 1 a. A 40 MHz processor was used to execute a program with the following instruction mix and clock cycle counts :

Instruction type	Instruction count	Clock cycle count
Integer arithmetic	45000	1
Data transfer	32000	2
Floating point	15000	2
Control transfer	8000	2

- Determine the i) effective CPI ii) MIPS Rate and iii) Execution time for this program. (06 Marks)
- b. Explain the Flynn's classification of computer architecture with block diagram. (08 Marks)
- c. Explain Implicit and Explicit parallelism. (06 Marks)
- 2 a. Explain the different types of data dependence. (08 Marks)
- b. Write the dependence graph for the following instructions :
- S1 : Load R1, A /  $R1 \leftarrow \text{Memory}(A)$  /
- S2 : Add R2, R1 /  $R2 \leftarrow (R1) + (R2)$  /
- S3 : Move R1, R3 /  $R1 \leftarrow (R3)$  /
- S4 : Store B, R1 /  $\text{Memory}(B) \leftarrow (R1)$  / (04 Marks)
- c. Explain Bernstein's conditions for parallelism. Detect the parallelism in the following code using Bernstein's conditions.
- P1 :  $C = D \times E$
- P2 :  $M = G + C$
- P3 :  $A = B + C$
- P4 :  $C = L + M$
- P5 :  $F = G \div E$ . (08 Marks)
- 3 a. Define Amdahl's law and explain in detail. Amdahl's law for fixed work load. (10 Marks)
- b. Explain : i) Average parallelism ii) Asymptotic speed up iii) System efficiency  
 iv) Redundancy and utilization. (10 Marks)
- 4 a. Compare CISC and RISC architectures in detail. (08 Marks)
- b. Explain the power architecture of IBM Rs 16000 super scalar processor. (08 Marks)
- c. Define : i) Instruction issue latency ii) Resource conflict iii) Scalar processor  
 iv) Vector processor. (04 Marks)
- 5 a. Explain : i) Internal data forwarding techniques ii) Possible hazards between read and write operations in instruction pipeline. (12 Marks)
- b. For the given reservation table below find :
- i) Forbidden latencies ii) Permissible latencies iii) Collision vector iv) State transition diagram v) Greedy cycles. (08 Marks)

		→ time					
		1	2	3	4	5	6
Stage	S1	X				X	
	S2			X			
	S3		X		X		X

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.  
 2. Any revealing of identification, appeal to evaluator and/or equations written eg. 42+8 = 50, will be treated as malpractice.

- 6 a. Explain different levels of memory hierarchy in detail. (10 Marks)  
b. Briefly explain different techniques to reduce miss rate and miss penalty. (10 Marks)
- 7 a. Explain context – switching policies in multithreaded architectures. (08 Marks)  
b. Explain KSR – 1 architecture with a slotted ring for communication in detail. (12 Marks)
- 8 Write short notes on the following :  
a. UMA model.  
b. Levels of parallelism in program execution.  
c. Synchronous and Asynchronous pipeline model.  
d. VLIW Architecture. (20 Marks)

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