05EC021

USN

NEW SCHEME

First Semester M.Tech. Degree Examination, Dec.06/Jan. 07

CMOS VLSI Design

Time: 3 hrs.] [Max. Marks:100

Note: *1. Answer any FIVE full questions.*
2. Assume missing data if any.
3. Draw neat diagrams where ever necessary.
4. Show complete solutions to the derivations/problems step by step.

1 a. Write an expression for threshold voltage of n channel E MOSFET and hence explain the significance of each term in this equation. Also explain the concepts of sub threshold voltage and sub threshold current. **(10 Marks)**

b. Draw a neat circuit of biased n channel E MOSFET operating in inversion mode and hence explain the concept of hot electron effect and punch through conditions, suggest any remedy if any to over come the problem of hot electron effect. **(10 Marks)**

2 a. Explain the transfer plot of CMOS inverter with necessary mathematical analysis for different values of $\beta n / \beta p$ ratios. **(10 Marks)**

b. Calculate the native threshold voltage for a n channel MOSFET at 300K for a process with a silicon substrate with $Na = 1.80 \times 10^{16}$, a SiO_2 gate oxide with thickness 200Å. Assume $\Phi_{ms} = -0.9$ volts, $Q_{fe} = 0$. **(10 Marks)**

3 a. With suitable mathematical analysis explain the transfer plot of MOS inverter with static load and pseudo n MOS inverter for different values of aspect ratios. **(10 Marks)**

b. Explain in detail the double metal MOS process rules for a VLSI technology. **(10 Marks)**

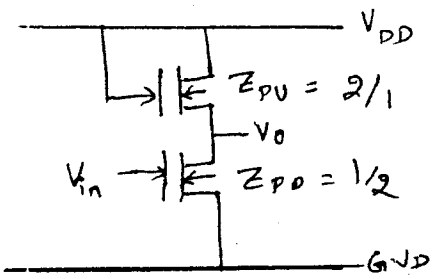
4 a. Describe in detail twin well CMOS process of fabrication. **(10 Marks)**

b. Calculate the time for free electrons to cross a n – channel E – MOSFET of channel length 3 microns. If Vdd = 5V, assume saturation velocity of electrons, $= V_n = 5 \times 10^7$ cm/sec and mobility of electrons = 800 $cm^2 / V - sec$. **(10 Marks)**

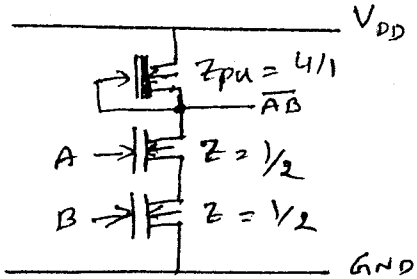
5 a. Show that as the RC delay lines approach infinity, the signal delay reduces when inverters are connected in cascade. **(10 Marks)**

b. Draw stick diagram for the following : **(10 Marks)**

(i)



(ii)



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6 a. With neat diagrams explain the construction and working principles of voltage bootstrapping synchronous dynamic circuit. (10 Marks)

b. Describe the construction and working principles of MOS differential amplifier driven by a constant current source and hence derive an expression for voltage gain of the amplifier. (10 Marks)

7 a. Describe with neat figures the fabrication of N WELL CMOS. (10 Marks)

b. Explain the operation of CMOS SR Latch and clocked JK Latch (10 Marks)

8 Write technical notes on the following :

a. SOS technology.

b. Clocked storage elements. (20 Marks)

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