CBCS SCHEME

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22LDE15

First Semester M.Tech. Degree Examination, Dec.2023/Jan.2024
Digital VLSI Design

Time: 3 hrs. Max. Marks: 100

Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.
2. M : Marks , L: Bloom's level , C: Course outcomes.

		Module – 1	M	L	C
Q.1	a.	Explain the operation of MOS with external bias.	10	L1	CO1
	b.	Obtain the basic current-voltage characteristics of an n-channel MOSFET.	10	L2	CO1
		OR			
Q.2	a.	Draw and explain the basic structure of the resistive – load inverter circuit.	6	L1	CO1
	b.	Write the equations of V_{OH}, V_{OL} and V_{IL} from the typical voltage transfer characteristics of resistive load inverter.	6	L2	CO1
	c.	Prove that depletion type nMOS transistor over come high stand by (DC) power dissipation when connected load.	8	L4	CO1
		Module – 2			
Q.3	a.	Explain the circuit operation of CMOS inverter circuit.	12	L3	CO2
	b.	Find the value of τ_{fall} and τ_{rise} of a typical inverter.	8	L4	CO2
		OR			
Q.4	a.	Calculate interconnect delay using i) RC Delay model ii) The Elmore delay.	10	L4	CO2
	b.	Write a note on switching power dissipation of CMOS inverters.	10	L6	CO2
		Module – 3			
Q.5	a.	Summarize the characteristics of memory devices.	8	L1	CO3
	b.	Explain the four transistor DRAM cell with two storage nodes.	6	L2	CO3
	c.	Explain the circuit topology of the CMOS SRAM cell.	6	L5	CO3
		OR			
Q.6	a.	Explain a three-transistor DRAM cell with the pull up and read/write circuitry.	10	L3	CO3
	b.	Draw and explain a 4-bit × 4-bit NAND based ROM array.	5	L5	CO3
	c.	Explain the hysteresis characteristics of a ferroelectric capacitor.	5	L1	CO3

		Module – 4			
Q.7	**a.**	Discuss the charge storage and charge leakage process in nMOS pass transistor.	**10**	**L2**	**CO4**
	b.	Implement the function $F = \overline{(A_1A_2A_3 + B_1B_2)}$ using dynamic CMOS logic gate.	**5**	**L4**	**CO4**
	c.	Realize Z = AB + (C + D) (E + F) + GH using standard CMOS logic.	**5**	**L4**	**CO4**
		OR			
Q.8	**a.**	Explain typical BiCMOS inverter circuit with four MOSFET and two BJT's.	**6**	**L1**	**CO4**
	b.	Explain the BiCMOS inverter circuit with i) Resistive base pull down ii) Active base pull down.	**8**	**L3**	**CO4**
	c.	Draw the circuit diagram of a BiCMOS NAND2 and NOR2 gate.	**6**	**L4**	**CO4**
		Module – 5			
Q.9	**a.**	Explain different models of ESD testing.	**6**	**L5**	**CO5**
	b.	Explain the design of tristable output circuit.	**6**	**L6**	**CO5**
	c.	Explain simple on-chip clock generation circuit using ring oscillator.	**8**	**L6**	**CO5**
		OR			
Q.10	**a.**	List and express the circuit parameter x_i occurring during manufacturing process and operating conditions.	**10**	**L6**	**CO5**
	b.	Explain the performance modeling procedure.	**10**	**L1**	**CO5**

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