CBCS SCHEME

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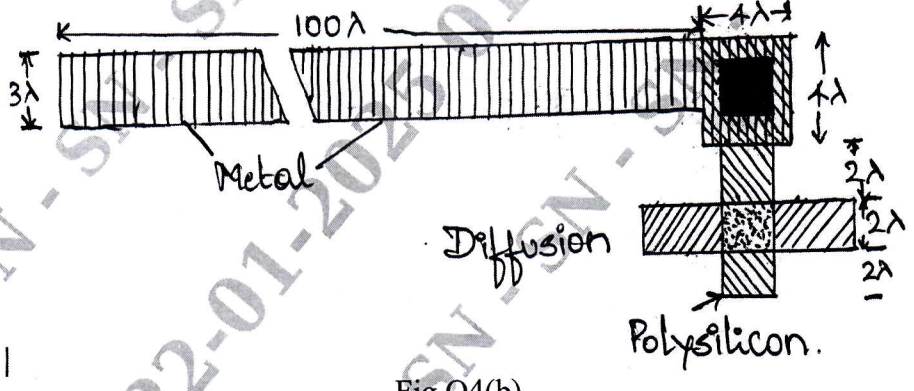
BEE515D

Fifth Semester B.E./B.Tech. Degree Examination, Dec.2024/Jan.2025
Fundamentals of VLSI Design

Time: 3 hrs. Max. Marks: 100

Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.
2. M : Marks , L: Bloom's level , C: Course outcomes.

		Module – 1	M	L	C
Q.1	a.	Demonstrate the steps involved in nMOS fabrication by out lining the key processes and illustrating necessary fabrication structures.	08	L3	CO1
	b.	Discuss Moore's law.	04	L2	CO1
	c.	Derive an expression for I_{ds} for both saturated and unsaturated regions.	08	L3	CO1
		OR			
Q.2	a.	Compare CMOS and Bi-polar technologies.	04	L2	CO2
	b.	Demonstrate your understanding of MOS transistor threshold voltage V_t by explaining its concept.	08	L3	CO2
	c.	Derive an expression for MOS transconductance, g_m.	08	L2	CO2
		Module – 2			
Q.3	a.	Outline the current versus input voltage characteristics of CMOS inverter with different regions.	06	L2	CO2
	b.	Define Z_{pu}/Z_{pd}. Show that pull up to pull down ratio for n-MOS inverter driven through one or more pass transistors is 8:1.	08	L3	CO3
	c.	Explain about the Latch-up effect in p-well structure.	06	L2	CO3
		OR			
Q.4	a.	Illustrate with neat circuit diagrams, different forms of pull-up.	06	L2	CO2
	b.	Calculate the total capacitance in pFarads between substrate and structure as shown in Fig.Q4(b) below for $\lambda = 5$ μm. Use standard values.  Fig.Q4(b)	08	L3	CO2
	c.	Estimate inverter delay in terms of Rise and Fall time.	06	L2	CO2
		Module – 3			
Q.5	a.	Derive scaling factors for any 10 device parameters.	10	L3	CO4
	b.	Explain about nMOS layout design rules.	05	L2	CO4
	c.	Construct a simple n-well based BiCMOS inverter stick diagram.	05	L3	CO4
		OR			
Q.6	a.	Examine the limitations of scaling in MOS technology by illustrating how subthreshold currents impose constraints.	10	L3	CO4
	b.	Briefly discuss about λ-based [Lambda] design rules and layout methodology.	05	L2	CO4
	c.	Construct a simple p-well CMOS inverter stick diagram.	05	L3	CO4

Module – 4					
Q.7	**a.**	Explain properties of pass transistors and transmission gate.	**06**	**L2**	**CO4**
	b.	Construct a 4 × 4 cross bar switch with neat diagram.	**08**	**L3**	**CO4**
	c.	Prove that for pseudo nMOS logic $Z_{pu}/Z_{pd} = 3/1$.	**06**	**L3**	**CO4**
OR					
Q.8	**a.**	Explain the concept of dynamic CMOS logic.	**06**	**L2**	**CO4**
	b.	Construct stick diagram and block diagram to explain the design approach of parity generator using nMOS logic.	**08**	**L3**	**CO4**
	c.	Develop a combinational circuit to generate two phase clocking.	**06**	**L3**	**CO4**
Module – 5					
Q.9	**a.**	Draw a neat diagram and explain the design of 4 bit serial- parallel multiplier.	**10**	**L2**	**CO4**
	b.	Construct CMOS stick diagram and explain the operation of three transistor dynamic RAM cell.	**10**	**L3**	**CO4**
OR					
Q.10	**a.**	With a neat diagram, explain the operation of 4 bit carry look ahead adder.	**10**	**L2**	**CO4**
	b.	Construct a JK flipflop circuit and outline its operation.	**10**	**L3**	**CO5**

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