CBCS SCHEME

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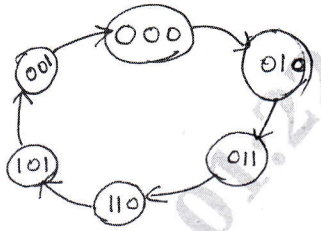
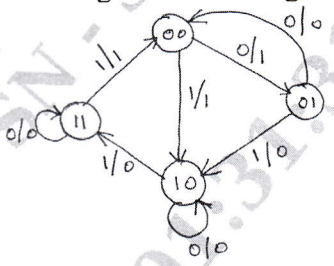
BEE306A

Third Semester B.E./B.Tech. Degree Examination, Dec.2024/Jan.2025
Digital Logic Circuits

Time: 3 hrs. Max. Marks: 100

Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.
2. M : Marks , L: Bloom's level , C: Course outcomes.

		Module – 1	M	L	C
Q.1	a.	Define combinational logic. What are Canonical forms in combinational logic? Explain the difference between SOP and POS canonical forms with suitable examples.	05	L1	CO1
	b.	What are prime implicant and essential prime implicant? Simplify the given Boolean function using KMap and identify its PI and EPI. $f(a,b,c,d) = \sum_m m(0,1,2,5,6,7,8,9,10,13,14,15)$	08	L2	CO1
	c.	Given $f(a,b,c) = \bar{a}b + ac + b\bar{c}$. Express it in canonical SOP and canonical POS.	07	L2	CO1
		OR			
Q.2	a.	Minimize the following expression in POS using K-map: $f(a,b,c,d) = \sum m(1,3,7,11,15) + \sum d(0,2,5)$	05	L3	CO1
	b.	Simplify the Boolean expression using K-map. $f(p,q,r,s,t) = \sum m(0,2,4,6,8,16,18,28,30) + dc(3,7,11,19,27,31)$	05	L3	CO1
	c.	Using Quine McCluskey and PI Reduction Table, determine minimal SOP for the function, $f(w,x,y,z) = \sum m(1,3,4,7,8,9,12,14) + \sum dc(2,13)$	10	L3	CO1
		Module – 2			
Q.3	a.	Write the Truth table for 8 line to 3 line priority Encoder.	04	L2	CO2
	b.	Write short note on look ahead carry adder.	06	L2	CO2
	c.	Design a combinational circuit to convert BCD to Excess 3 code.	10	L3	CO2
		OR			
Q.4	a.	Design full adder using a decoder (74138).	05	L3	CO2
	b.	Implement the following function using 8 : 1 MUX. Treat w, x, y as select lines, $f(w,x,y,z) = \sum m(0,1,5,6,7,9,10,15)$.	05	L3	CO2
	c.	Implement 2 bit comparator using 4-16 decoder.	10	L3	CO2
		Module – 3			
Q.5	a.	With the help of logic diagram, explain the working of Master Slave JK flipflop and explain how race around condition is eliminated.	10	L2	CO3
	b.	Explain how SR flip flop/latch act as switch debouncing circuit and draw its waveform.	06	L2	CO3
	c.	Differentiate between latch and flip flop.	04	L2	CO3
		OR			
Q.6	a.	Derive the characteristics equation of SR, JK and T flip flop.	06	L3	CO3
	b.	With a logic diagram, explain the working of SR-flip flop.	07	L2	CO3
	c.	With the help of logic diagram, explain the working of positive edge Triggered D-flip flop.	07	L2	CO3

		Module – 4			
Q.7	**a.**	Design a synchronous counter for the following sequence using JK flip flop.  Fig. Q7 (a)	**10**	**L3**	**CO4**
	b.	Design synchronous MOD-6 counter using clocked T flip flop.	**10**	**L3**	**CO4**
		OR			
Q.8	**a.**	Design 4 bit register using positive edge triggered DFF to operate as below : Mode A_1 / Select A_0 / Register operation 0 0 → Hold 0 1 → Shift Right 1 0 → Shift Left 1 1 → Parallel load	**12**	**L4**	**CO4**
	b.	Explain 4 bit SISO uni-directional shift register using DFF (Consider positive edge triggered).	**08**	**L2**	**CO4**
		Module – 5			
Q.9	**a.**	Design a sequential circuit using TFF for the figure shown in Fig. Q9 (a).  Fig. Q9 (a)	**12**	**L3**	**CO5**
	b.	With a neat diagram, explain mealy and Moore model in a sequential circuit analysis.	**08**	**L2**	**CO4**
		OR			
Q.10	**a.**	Write short note on : (i) Read / write memories (ii) Programmable ROM	**10**	**L2**	**CO6**
	b.	Write short note on : (i) Flash memory (ii) EPROM	**10**	**L2**	**CO6**

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