CBCS SCHEME

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18EE34

Third Semester B.E. Degree Examination, Dec.2024/Jan.2025
Analog Electronic Circuits

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Write a Diode circuit which clips the voltage above +7V and below +4V. Explain its operation with input voltage of 15 sinwt. Write input and output voltage waveform and also transfer characteristics. Assume Ideal Diode. **(06 Marks)**

b. Analyze collector-to-base Bias circuit to obtain expressions for I_B, I_c and V_{CE} and there by derive an expression for S_{ICO}. **(06 Marks)**

c. A voltage divider Bias circuit has upper Resistor R_1 = 18 kΩ, lower Resistor R_2 = 2 kΩ, R_C = 10 kΩ, R_E = 1 kΩ, V_{CC} = 20 V, and β = 100. Using exact analysis, find V_C, V_{CE}, I_C and V_{CB}. Indicate the operating region. **(08 Marks)**

OR

2 a. Write the circuit which clamps Negative peak of 16V peak-to-peak square wave to -2V. Explain its operation with input and output waveforms. Assume Ideal Diode. **(06 Marks)**

b. Design Emitter stabilized bias circuit using V_{CC} = 20V, V_{CEQ} = ½ V_{CC}, I_{CQ} = 3mA, β = 100, $R_C = 5R_E$. Write the circuit. **(07 Marks)**

c. Write transistor switching circuit and explain the switching characteristics of transistor with graph. **(07 Marks)**

Module-2

3 a. Using h-parameter equation, define h-parameter for a 2-port network and write h-model. **(06 Marks)**

b. State and prove Miller's Theorem. **(06 Marks)**

c. Transistor used in amplifier circuit show in Fig Q3(c), has h_{ie} = 1.1 kΩ, h_{fe} = 50, h_{ce} = 0, h_{re} = 0. Find A_I, Z_{in}, Z_0 $A_V = \frac{V_0}{V_{in}}$ & $A_{VS} = \frac{V_0}{V_S}$.

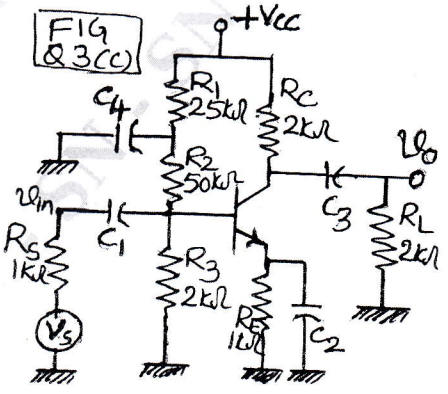

Fig Q3(c) **(08 Marks)**

OR

4 a. For the 2-port network shown in Fig Q4(a), derive an expression for A_I, Z_{in} A_V and Z_0 interms of h-parameters, R_S and R_L.

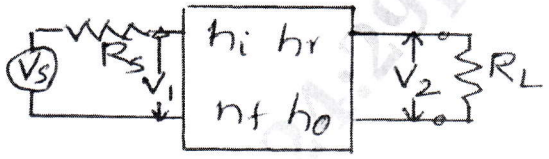

Fig Q4(a) **(06 Marks)**

b. Using simplified (approx) h-model of CE configuration, analyze common base amplifier to derive an expression for A_I, Z_{in}, A_V and Z_0. **(07 Marks)**

c. Transistor used in RC coupled CE amplifier with fixed Bias has h_{ie} = 1 kΩ, h_{fe} = 60, h_{oe} = 15 μA/V, h_{re} = $2*10^{-4}$. Calculate has R_S = 1 kΩ, R_B = 56 kΩ, R_C = 10 kΩ and R_L = 10 kΩ. Find A_I, A_{IS} Z_{in} and Z_0. **(07 Marks)**

Module-3

5 a. Explain why cascading is required. Write Block diagram of 4-stage cascaded amplifier and derive an expression for overall gain of the system in-terms of individual gains. **(06 Marks)**

b. With the help of circuit diagram and waveforms explain Darlington Emitter follower. Mention two important features of this circuit. **(06 Marks)**

c. With the help of block diagram, briefly explain Negative Feed Back System. What are the advantages of Negative Feed Back in Amplifier? **(08 Marks)**

OR

6 a. Derive an expression for output impedance in voltage shunt Feed Back and Input Impedance in voltage series Feed Back amplifiers. **(08 Marks)**

b. An amplifier with Negative Feed Back has closed loop gain of 20. An input of 50 mV is required to produce certain output without Feedback, write 0.5V input is required to produce same output with Negative Feedback. Find open loop gain and Feed Back factor. **(05 Marks)**

c. Two amplifiers are cascaded with R_L = 20 kΩ, R_S = 2 kΩ
Stage 1 : No load Gain = 1, Input Impedance = 500 kΩ, Output Impedance = 1 kΩ
Stage 2 : No-load gain = 300, Input Impedance = 1 kΩ, output Impedance = 50 kΩ
Find i) loaded gain of each stage ii) current gain of cascaded system iii) total overall voltage gain of cascaded system with R_S(V_L/V_S). **(07 Marks)**

Module-4

7 a. With a circuit, Graph/waveform, explain the operation of class 'B' push pull amplifier. Show that maximum conversion efficiency is 78.5%. **(08 Marks)**

b. A series fed class A power amplifier shown in Fig Q7(b) has input voltage generating ac base current of 12mA (Max). Find input power, output power, efficiency and power dissipated.

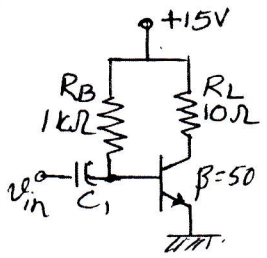

Fig Q7(b) **(05 Marks)**

c. Write the circuit of Wien Bridge oscillator and derive an expression for output frequency. **(07 Marks)**

OR

8 a. State Barkahusen criterion for sustained oscillations. Explain with circuit, how Barkhausen criterion is met in RC-phase shift oscillator. **(08 Marks)**

b. Class B complementary power amplifier has a supply of ± 15V and load of R_L = 10Ω. Find :

i) Maximum ac power developed and the efficiency under maximum ac power condition

ii) Maximum power dissipated per transistor and the efficiency under Max. Power dissipation condition. **(06 Marks)**

c. Briefly explain electrical equivalent of a crystal. A crystal has L = 1 H, C = 0.01 pF, C_m = 1 pF, R = 2 kΩ. Find series and parallel Resonant frequency and Q-factor. **(06 Marks)**

Module-5

9 a. With circuit and small signal model of common source JFET amplifier using Fixed bias, derive an expression for Z_{in}, Z_0 and A_V. **(06 Marks)**

b. Explain the construction, working and characteristics of n-channel depletion type MOSFET. **(08 Marks)**

c. For circuit shown in Fig Q9(c), find $V_{GS(Q)}$, V_{DSQ} V_S, V_G, I_{DQ} and V_D.

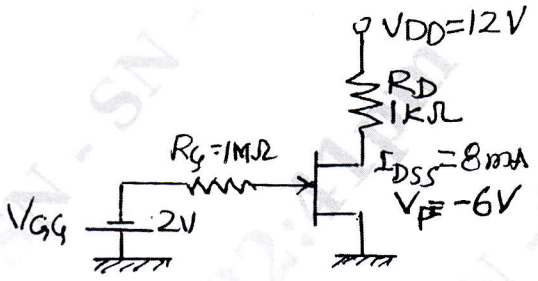

Fig Q9(c) **(06 Marks)**

OR

10 a. Compare JFET over MOSFET and BJT over MOSFET. **(06 Marks)**

b. Explain the construction, working and characteristics of n-channel JFET with neat sketch and graph. **(07 Marks)**

c. For the circuit, shown in Fig Q10(c), find g_m, r_d, z_{in}, z_0, A_v. Write small signal model. Take $V_{GS(Q)} = V_{GG}$ = -2V

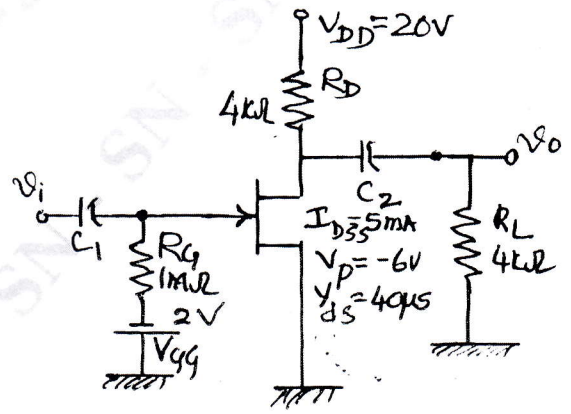

Fig Q10(c) **(07 Marks)**

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