

# CBCS SCHEME

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21EC63

Sixth Semester B.E./B.Tech. Degree Examination, Dec.2024/Jan.2025

## VLSI Design and Testing

Time: 3 hrs.

Max. Marks: 100

*Note: Answer any FIVE full questions, choosing ONE full question from each module.*

### Module-1

- 1 a. Realize the CMOS compound gate for the following functions:  
(i)  $Y = \overline{ABC + D}$  (ii)  $Y = A(B + C) + \overline{DE}$  (08 Marks)  
b. Implement a positive edge triggered D flip flop using transmission gate and write the necessary timing diagram. (08 Marks)  
c. Analyze the working of tristate inverter. (04 Marks)

OR

- 2 a. Draw the circuit diagram of CMOS inverter and derive its transfer characteristics by graphical method. (06 Marks)  
b. Derive the equation for drain current of a MOSFET in non-saturated and saturated region of operation. (10 Marks)  
c. Explain the following non-ideal effects of MOSFETs:  
(i) Channel length modulation (ii) Mobility degradation. (04 Marks)

### Module-2

- 3 a. With neat diagrams, explain the complete CMOS n-well fabrication process. (10 Marks)  
b. Draw the layout diagram for the following function and also estimate the area.  
 $Y = \overline{(A + B + C)D}$  (10 Marks)

OR

- 4 a. Using Elmore delay model estimate the  $t_{pdf}$  and  $t_{pdr}$  of a 3-input NAND gate if the output is loaded with 'h' identical gates. (08 Marks)  
b. Find the logical effort and parasitic delay of (i) 2 input NOR gate and (ii) 3-input NAND gate. (06 Marks)  
c. Construct necessary equivalent circuit for the computation of  $t_{pdf}$  of an inverter driving another inverter using RC delay model. (06 Marks)

### Module-3

- 5 a. With necessary circuit diagrams explain the operation of (i) 4 transistor DRAM and (ii) 3 transistor DRAM cells. (10 Marks)  
b. Explain the operation of full CMOS SRAM cell with necessary circuit topology. (06 Marks)  
c. Explain the hysteresis characteristics of ferroelectric capacitor with necessary diagram. (04 Marks)

OR

- 6 a. Explain the operation of 4×4 NOR based ROM array with necessary circuit diagram. (08 Marks)  
b. With necessary circuit diagram and bias conditions, explain the operation of NOR flash memory. (06 Marks)  
c. Explain binary tree based column decoder design with necessary diagram. (06 Marks)

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.  
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8=50, will be treated as malpractice.

**Module-4**

- 7 a. Differentiate between fault and failure with an example. Explain different types of stuck at fault with example. (06 Marks)
- b. Explain feedback bridging fault with an example. (06 Marks)
- c. For the circuit shown in Fig.Q7(c), using Boolean difference (i) detect s-a-0 and s-a-1 at  $x_1$ , (ii) determine partial Boolean difference for  $x_2 - l - n - p - F$ .

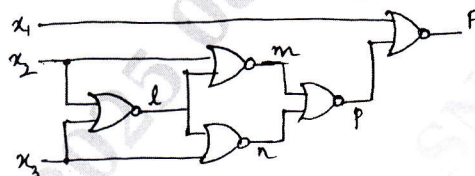


Fig.Q7(c)

(08 Marks)

**OR**

- 8 a. What is fault diagnosis? Explain delay fault detection with an example. (08 Marks)
- b. Find the test pattern for line 6 s-a-0 for the circuit shown in Fig.Q8(b) using D algorithm.

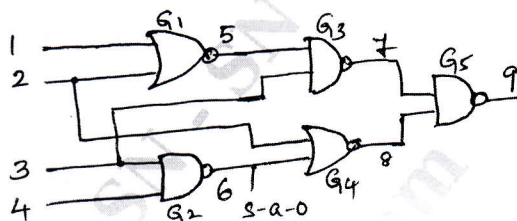


Fig.Q8(b)

(12 Marks)

**Module-5**

- 9 a. For the state table shown in Table Q9(a), find  
(i) Response for 010 sequence, (ii) Homing tree, (iii) Distinguishing tree.

Present State	Input	
	$x = 0$	$x = 1$
A	B, 0	D, 0
B	A, 0	B, 0
C	D, 1	A, 0
D	D, 1	C, 0

Table Q9(a)

(10 Marks)

- b. Write a note on functional fault model to detect faults in sequential circuits. (05 Marks)
- c. Explain the process of testing sequential circuit as iterative combinational circuits. (05 Marks)

**OR**

- 10 a. Define the terms controllability and observability with an example. (05 Marks)
- b. With a neat logic diagram, explain clocked hazard free latches used in LSSD technique. (08 Marks)
- c. Explain partial scan technique using system clock with necessary diagram. (07 Marks)

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