CBCS SCHEME

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BEC306C

Third Semester B.E./B.Tech. Degree Examination, Dec.2024/Jan.2025
Computer Organization and Architecture

Time: 3 hrs. Max. Marks: 100

Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.
2. M : Marks , L: Bloom's level , C: Course outcomes.

			M	L	C
		Module – 1			
Q.1	a.	With neat diagram explain connection between the processor and memory.	10	L1	CO1
	b.	Write the difference between little endian and big endian memory assignments.	05	L1	CO1
	c.	Write a short note on basic performance equation.	05	L1	CO1
		OR			
Q.2	a.	Describe the concept of branching with an example program of instruction execution.	10	L1	CO1
	b.	Represent the following decimal values as signed 7-bit numbers using sign and magnitude, signed 1's complement and signed 2's complement formats. – 55, +51, 8, – 27, – 39, +43, – 10, 62	05	L2	CO1
	c.	Write a short note on memory operations.	05	L1	CO1
		Module – 2			
Q.3	a.	What is an addressing mode? Explain any four types of addressing modes, with suitable example.	10	L1	CO2
	b.	Write a program to compute the sum of test scores of all the students in the three tests. Store the corresponding sums in memory.	10	L2	CO2
		OR			
Q.4	a.	Explain the Rotate and Shift instructions with an example.	10	L1	CO2
	b.	Define subroutine. Explain subroutine linkage using a link register.	05	L1	CO2
	c.	What are assembler directives? Explain any two directives.	05	L1	CO2
		Module – 3			
Q.5	a.	Define I/O interface? Explain I/O interface to connect an input device to the bus with neat diagram.	10	L1	CO3
	b.	What is interrupt? Discuss interrupt I/O method for data transfer.	05	L1	CO3
	c.	Describe two methods of handling multiple devices.	05	L1	CO3
		OR			
Q.6	a.	Explain the use of DMA controllers in a computer system with neat diagram.	10	L1	CO3
	b.	Write a note on Bus Arbitration.	10	L1	CO3
		Module – 4			
Q.7	a.	Explain the organization of 1K×1 memory chip.	10	L1	CO4
	b.	Write a note on : (i) Static memories (ii) Cache memory	10	L1	CO4
		OR			
Q.8	a.	Explain the Magnetic disk principles.	10	L1	CO4
	b.	Draw and explain the internal organization of 2M×8 asynchronous DRAM chip.	10	L2	CO4
		Module – 5			
Q.9	a.	Discuss with neat diagram the single bus organization of data path inside a processor.	10	L1	CO5
	b.	What are the actions required to execute a complete instruction ADD (R_2), R_1	10	L1	CO5
		OR			
Q.10	a.	Draw and explain multiple bus organization of CPU.	10	L1	CO5
	b.	Draw and explain organization of the control unit to allow conditional branching in the microprogram.	10	L1	CO5

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