CBCS SCHEME

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18CS34

Third Semester B.E. Degree Examination, Dec.2024/Jan.2025
Computer Organization

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. With a neat diagram, explain the basic operational concepts of a computer. **(06 Marks)**

b. Explain the basic instruction types with example. **(08 Marks)**

c. Explain Big Endian and Little Endian methods by addressing with proper example. **(06 Marks)**

OR

2 a. Define addressing mode. Explain the following addressing modes with suitable examples :
(i) Register
(ii) Direct
(iii) Indirect
(iv) Auto-Increment **(10 Marks)**

b. Explain SPEC rating of a computer. **(05 Marks)**

c. Write an assembly program to add numbers stored in consecutive memory locations as Num_1, Num_2..... Num_n and store the result at location SUM by using branching technique. **(05 Marks)**

Module-2

3 a. What is DMA? Explain it's operation using registers in a DMA interface. **(08 Marks)**

b. Explain the following interrupt nesting methods :
(i) Daisy chain.
(ii) Implementation of interrupt nesting. **(06 Marks)**

c. What is DMA Bus Arbitration? Explain Distributed arbitration with neat diagram. **(06 Marks)**

OR

4 a. Explain the I/O interface for an input device (key board) interface to the processor with a neat block diagram. **(08 Marks)**

b. Explain synchronous Bus with neat timing diagram. **(06 Marks)**

c. With neat diagram, explain USB split bus operation. **(06 Marks)**

Module-3

5 a. With a neat diagram, explain the internal organization of $2M \times 8$ DRAM chip. **(10 Marks)**

b. Explain Direct Mapping function. **(05 Marks)**

c. Explain the read and write operation in a single SRAM cell with circuit diagram. **(05 Marks)**

OR

6 a. With neat diagram, explain the memory hierarchy with respect to speed, size and cost. **(05 Marks)**

b. With neat circuit diagram, explain how data are written into ROM. **(05 Marks)**

c. What is memory interleaving? Explain with a suitable example. **(10 Marks)**

Module-4

7 a. Explain the design of a 4-bit carry look ahead adder. Calculate number of gate delays for S_3 and C_4. **(08 Marks)**

b. With neat diagram, explain binary addition/Subtraction. **(06 Marks)**

c. Multiply (+14) and (-6) using Booth's algorithm. **(06 Marks)**

OR

8 a. Perform bit pair recoding for -11 and +27 [(-11) multiplicand and (+27) multiplier]. **(06 Marks)**

b. Perform the following operations on the 5-bit signed numbers using 2's complement representation system. Further indicate whether overflow has occurred :

(i) (-10) + (-13)

(ii) (+10) – (+14)

(iii) (+7) – (-15) **(06 Marks)**

c. Perform 1100÷11 using non restoring division algorithm. **(08 Marks)**

Module-5

9 a. With neat diagram, explain the working of single-bus organization of the datapath inside processor. **(08 Marks)**

b. Write the sequence of control steps for the execution of an instruction Add (R_3), R_1. **(07 Marks)**

c. Write the control sequence for the execution of an unconditional branch instruction. **(05 Marks)**

OR

10 a. With neat diagram, explain the organization of Hardwired control unit. **(07 Marks)**

b. What is pipelining? Explain the 4-stage pipeline. **(05 Marks)**

c. With neat diagram, explain the Three-bus organization of the datapath. **(08 Marks)**

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