(04 Marks) (08 Marks)

## CBCS SCHEME

USN		18EE46
	Fourth Semester B.E. Degree Examination, July/August 2022	
	Operational Amplifiers and Linear IC's	
Tin	3 hrs. Max. Mark	s: 100
	Note: Answer any FIVE full questions, choosing ONE full question from each mode	ule.
	Module-1	
1	<ul> <li>Explain the working of Op – Amp as non – inverting amplifier. Derive the express voltage gain.</li> <li>An Input of 3V is Fed to the non inverting terminal of an Op – Amp. The amp</li> </ul>	08 Marks)
	OR	
2	Draw and explain the 2 input inverting summing amplifier and derive its output equation Vo. Also explain how to convert it to an averaging amplifier.	08 Marks)
	Module-2	
3	Explain Working and design of voltage follower Regulator.  Design a First Order Low Pass filter with a cut off frequency of 1KHz and Pass 1	10 Marks) 06 Marks)
		Ŷ,
4	OR  Draw the First Order High Pass Butterworth filter and obtain its Frequency Response	se. 10 Marks)
	. With a neat circuit diagram, explain the Adjustable Voltage Regulator and its Opera	ition.
9	Find the Range in which output voltage can be varied with the help of 317 IC	06 Marks) Regulator 04 Marks)
	Module-3	
5	Draw and explain the Operation of Non Inverting Zero Crossing detectors.  Explain the working of voltage to current converter with grounded load.	08 Marks) 04 Marks) 08 Marks)
_	OR	T Schmitt
6	With a neat circuit diagram and waveforms, explain the Operation of inverting	08 Marks)

b. Give comparison between Schmitt trigger and Comparator.
c. Explain the working of R - C phase shift oscillator using Op - Amp.

Module-4

- 7 a. With a neat circuit diagram, explain the Operation of Non Saturating precision half Wave Rectifier. (10 Marks)
  - b. Explain the working of Successive Approximation Type ADC with neat sketch. (10 Marks)

## OR

- 8 a. Explain the Operation of R 2R ladder digital to Analog Converter Circuit. (10 Marks)
  - b. With a neat circuit diagram, explain the working of Precision full wave Rectifier. (10 Marks)

## Module-5

- 9 a. Draw the basic block diagram of Phase Locked Loop (PLL) and explain its each component.
  (10 Marks)
  - b. With a neat diagram, explain the Internal Architecture of IC 555 Timer. (10 Marks)

## OR

- 10 a. Draw and explain working of Monostable Multivibrator using 555 Timer and draw its Input Output wave forms. (12 Marks)
  - b. Define the following terms related to PLL:
    - i) Lock range ii) Capture range iii) Pull in Time iv) Tracking range.

(08 Marks)