USN | | | | | | | | | | |

**NEW SCHEME**

# M.Tech. Degree Examination, May / June 2006

## CMOS VLSI Design

Time: 3 hrs.] [Max. Marks:100

**Note:** ***Answer any FIVE full questions.***

1 a. Explain the trends in transfer characteristics with $\beta_n/\beta_p$ ratio's, using suitable mathematical analysis. **(10 Marks)**

b. Write an expression for threshold voltage of n - channel E-MOSFET and hence explain the role of each term in the equation. Modify this equation suitably so as to express the same for $V_{SB} = 0$ **(10 Marks)**

2 a. Estimate the ON state resistance of the inverter circuit shown in figure 2(a), using the concepts of sheet resistance. Assume 5 $\mu$ m technology. Given the following data, also estimate current between power lines. Derive the formula used for calculations.

| LAYER | $R_S$ ohm per square | | |
|---|---|---|---|
| | 5 $\mu$ m | orbit | orbit 1.2 $\mu$ m |
| n-transistor channel | $10^4$ | $2 \times 10^4$ | $2 \times 10^4$ |
| p-transistor channel | $2.5 \times 10^4$ | $4.5 \times 10^4$ | $4.5 \times 10^4$ |

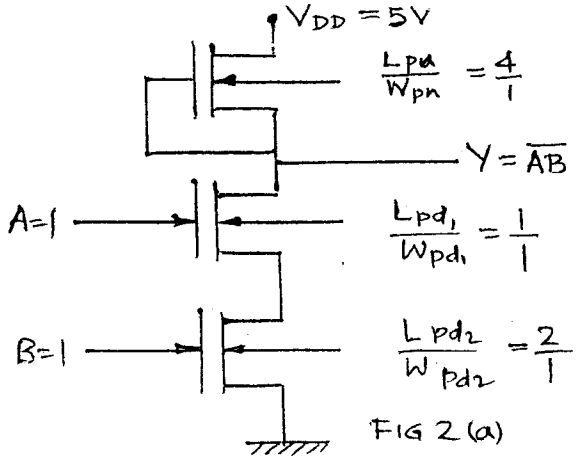

FIG 2(a)

**(10 Marks)**

b. Explain the significance of channel length modulation and hot electron effect in MOS devices. **(10 Marks)**

3 a. Explain the operation of MOSFET in CS configuration when the load to the devices are i) Resistive load, ii) Diode – connected load, iii) Current source load. **(15 Marks)**

*Contd...2*

b. For the circuit shown in figure 3(b), calculate the small signal voltage gain of the circuit.

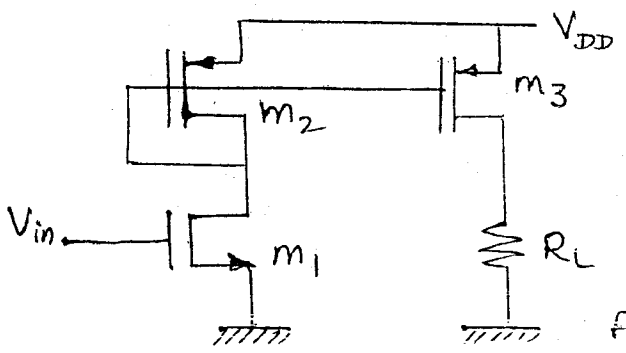


Fig 3(b)

(05 Marks)

4 a. Explain the fabrication process of P well CMOS inverter with neat sketches where ever necessary. (10 Marks)

b. What are lambda based design rules? Bring out the merits and demerits there of. (10 Marks)

5 a. Draw symbol diagram of a two bit CMOS shift registers, reducing the number of transistors wherever possible. (10 Marks)

b. Draw nMOS, CMOS version of the circuit to realise the boolean expression.

$$Z = \overline{(D+E+A)(B+C)}$$

(10 Marks)

6 a. Derive an expression for figure of merit of n channel E-MOSFET. (10 Marks)

b. Explain the working of CMOS transmission sate with its equivalent resistance curve. What are the advantages of transmission gate ? (10 Marks)

7 a. What is domino CMOS logic? Compare it with conventional CMOS logic. Justify the same with one example each. (10 Marks)

b. Explain how clock signal can be generated, distributed and stored in dynamic CMOS inverter circuits. (10 Marks)

8 Write technical note on the following :

a. Bi-CMOS inverter

b. Pass transistor circuit

c. Punch through conditions in MOS transistor.

d. CMOS D latch. (20 Marks)

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