E/b/4

USN | | | | | | | | | | C021

NEW SCHEME

First Semester M.Tech. Degree Examination, June 2007
CMOS VLSI Design

Time: 3 hrs.] [Max. Marks:100

Note : ***Answer any FIVE full questions.***

1 a. Starting from the fundamentals, derive an expression for threshold voltage in a MOS transistor. **(06 Marks)**

b. Briefly explain the following terms: i) Channel length modulation ii) Fowler – Nordheim tunneling iii) Impact ionization. **(08 Marks)**

c. With a neat diagram showing the levels of various voltages and transfer characteristic explain the noise margin. **(06 Marks)**

2 a. Explain the working of differential inverter with a neat diagram and the transfer characteristics. **(06 Marks)**

b. With respect to: i) Change in control input ii) Change in switched input, explain the transmission gate output characteristics. **(06 Marks)**

c. Discuss the various circuit arrangements to be employed in BICMOS inverters. **(08 Marks)**

3 a. Explain with neat sketches the lambda bared design rules with respect to wires, transistors and contacts. **(08 Marks)**

b. With a neat structure (final diagram) explain the twin-tub CMOS process. **(06 Marks)**

c. Bring out the differences between metal interconnect and polysilicon / refractory metal interconnect. **(06 Marks)**

4 a. Show that the transit time and time delay are interchangeable in CMOS technology. **(08 Marks)**

b. Derive an expression for total delay when number of stages N is odd and even while driving large capacitive loads. **(08 Marks)**

c. Draw the CMOS circuit diagram and the stick diagram for a 2 input NAND gate. **(04 Marks)**

5 a. With a neat CMOS circuit diagram showing the parasitic capacitance explain 2 input CMOS NOR gate and specify the condition for K_n and K_p to get $V_{th} = V_{DD}/2$. **(07 Marks)**

b. Bring out the differences between AND-OR-inverter (AOI) logic and OR-AND-inverter (O-A-I) logic with a suitable example. **(06 Marks)**

c. Explain briefly the SR latch with gate level schematic truth tables and CMOS circuit. **(07 Marks)**

6 a. Explain the phenomenon of charge storage and charge leakage and obtain the expression for the holding time t_{hold}. **(07 Marks)**

b. Dynamic CMOS logic circuits cannot be cascaded. Why? Explain. **(06 Marks)**

c. Discuss the pipelined NORA CMOS system with relevant diagrams. **(07 Marks)**

7 a. Explain the differential amplifier with a neat CMOS circuit and cross-section. Obtain the expression for transconductance of differential amplifier. **(10 Marks)**

b. Starting from the fundamentals derive an expression for the reference voltage V_{REF} in a conventional CMOS band gap reference. **(10 Marks)**

8 a. Explain the latch up phenomenon in a CMOS structure with the help of cross sectional view, circuit model and V-I characteristics. **(08 Marks)**

b. Bring out the differences between NMOS and CMOS fabrication processes. **(05 Marks)**

c. Explain the various techniques employed for generation of clock in CMOS technology. **(07 Marks)**