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NEW SCHEME

05EC021

Reg. No. | | | | | | | | | | |

First Semester M.Tech. Degree Examination, January/February 2006

LDS/LEC/LVS/LPE/LIE/LEL

CMOS VLSI Design.

Time: 3 hrs.) (Max.Marks : 100

Note: *Answer any FIVE full questions.*

1. (a) Describe the working on nMOS enhancement mode transistor with diagrams and output characteristics. **(8 Marks)**

   (b) Deduce high frequency small signal equivalent circuit of MOS transistor and an expression for figure of merit. **(6 Marks)**

   (c) What are the advantages of BiCMOS inverter over CMOS counterparts? Draw the circuit diagram of a BiCMOS inverter in which problems associated with static power dissipation and stored charge in the base are eliminated and explain its working. **(6 Marks)**

2. (a) Explain λ based design rules as applicable to MOS layers and transistors. **(8 Marks)**

   (b) Compare CMOS and SOI technology. Draw sketches involved in CMOS inverter fabrication process. **(6 Marks)**

   (c) Define sheet resistance, standard unit of capacitance and delay unit of time. **(6 Marks)**

3. (a) Show that nMOS/CMOS inverter pair delay is invariant. **(6 Marks)**

   (b) A MOS layer is 5λ wide, 60λ long and $1\mu m$ thick. The resistivity of the layer is $1\Omega cm$. Using sheet resistance concept, calculate the resistance of the MOS layer along its length. **(6 Marks)**

   (c) An off chip capacitance load of 20 pF is to be driven by a chain of CMOS inverters of 5μ technology. Compute the number of inverters, width factor and over all delay through the chain for minimum overall delay. Assume C_g for $5\mu m$ technology as 0.01pF and $R_s = 10k\Omega$. **(8 Marks)**

4. (a) Derive an expression for the propagation delay through a chain of pass transistors. **(6 Marks)**

   (b) Draw circuit and stick diagrams of two input NOR gate and 1 bit shift register using CMOS inverters. Standard colour/monochrome codes are to be used for stick diagrams. **(8 Marks)**

   (c) Derive scaling factors of the following MOS parameters using combined voltage and dimension scaling model :

   i) Number of gates - N

   ii) Saturation current - I_{dss}

   iii) Power speed product - P_T **(6 Marks)**

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5. (a) Distinguish between combinational and sequential circuits. (4 Marks)

(b) Describe the behaviour of two inverter bistable element with one inveter in the feed back loop. Also derive expressions for output voltages of inverters. (10 Marks)

(c) Differentiate between static and dynamic CMOS circuits with relevant diagrams. (6 Marks)

6. (a) Explain how domino circuits evolved from dynamic CMOS circuits and reasons there of. (6 Marks)

(b) Draw nMOS and CMOS version of the circuit to realise the following Boolean expression : (8 Marks)

$z = \overline{A(D+E)+BC}$.

(c) Explain the working of clocked SR latch with the help of circuit diagram and waveforms. (6 Marks)

7. (a) What is latch up in CMOS inverters and how is it minimised? (6 Marks)

(b) Realise NOR and NAND gate functions using transmission gates. (8 Marks)

(c) What are the demerits of n and p pass transistors w.r.t output voltages and how are these overcome in a transmission gate? (6 Marks)

8. Write short notes on :

(a) MOS model

(b) Differential amplifier

(c) Clock generation and distribution

(d) Voltage boot strapping. (4×5=20 Marks)

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