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05EC021

M.Tech. Degree Examination, Dec. 07 / Jan. 08
CMOS VLSI Design

Time: 3 hrs. Max. Marks:100

Note : ***Answer any FIVE full questions.***

1 a. Briefly explain the second order effects in MOSFET. **(07 Marks)**

b. With neat diagram and transfer characteristics, explain the CMOS inverter. Obtain the necessary expressions for the same. **(08 Marks)**

c. Calculate the native threshold voltage for an n-transistor at 300^0 k for a process with a silicon substrate with $N_A = 1.8 \times 10^{16}$ /cc, $t_{ox} = 200\,\text{Å}$. Assume $\phi_{ms} = -0.9V$, $Q_{fc} = 0$, $\eta_I = 1.45 \times 10^{10}$ /cc. **(05 Marks)**

2 a. With relevant response curves, explain the transmission gate output characteristics for change in control input and for change in switched input. **(06 Marks)**

b. Obtain the scaling factors for the following – i) Gate delay ii) Current density iii) Switching energy. **(06 Marks)**

c. With neat fabrication sketches. Explain the silicon on insulator (SOI) COMS process. **(08 Marks)**

3 a. Explain the CMOS process enhancement with reference to i) metal interconnect ii) polysilicon /refractory metal inter connect. **(06 Marks)**

b. For the following structure obtain values for Cm, Cp, Cg and C_T. Given that the relative values of capacitances are metal 1 = 0.075 □ Cg, polysilicon = 0.1 □ Cg.

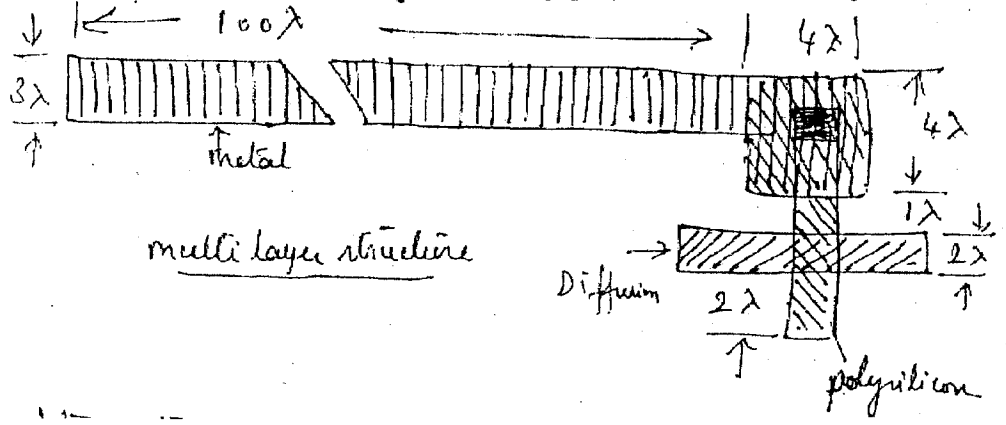

Fig. Q 3(b) **(08 Marks)**

c. Obtain the CMOS circuit and stick diagram for the following function $f = \overline{(A+BC)D}$. **(06 Marks)**

4 a. With a neat diagram, obtain the parasitic device capacitance in CMOS 2 input NOR gate for kN = 4 KP and explain the circuit operation. **(06 Marks)**

b. Differentiate between AOI logic and OAI logic with a suitable example of each. **(08 Marks)**

c. For the given function F = AB + A'C' + AB'C obtain the i) CMOS TG realization
ii) COMS transistor realization. **(06 Marks)**

5 a. With a neat gate level schematic and CMOS circuit explain the CMOS SR latch circuit based on clocked NOR2 gates. (06 Marks)

b. Briefly discuss the charge storage and charge leakage in n mos pass transistor. (06 Marks)

c. Calculate the worst case time for the following data given $V_{TO} = 0.8$ V, $\nu = 0.4\ V^{1/2}$, $|2\phi_F| = 0.6V$, $C_{OX} = 0.065$ f F /μ m^2, $C^1_{metal} = 0.036fF/\mu m^2$, $C^1_{poly} = 0.055fF/\mu m^2$, $C_{jo} = 0.095$ f F/μ m^2, $C_{josw} = 0.2$ f F/μ m. $I_{leakage} = 0.85$ pA.

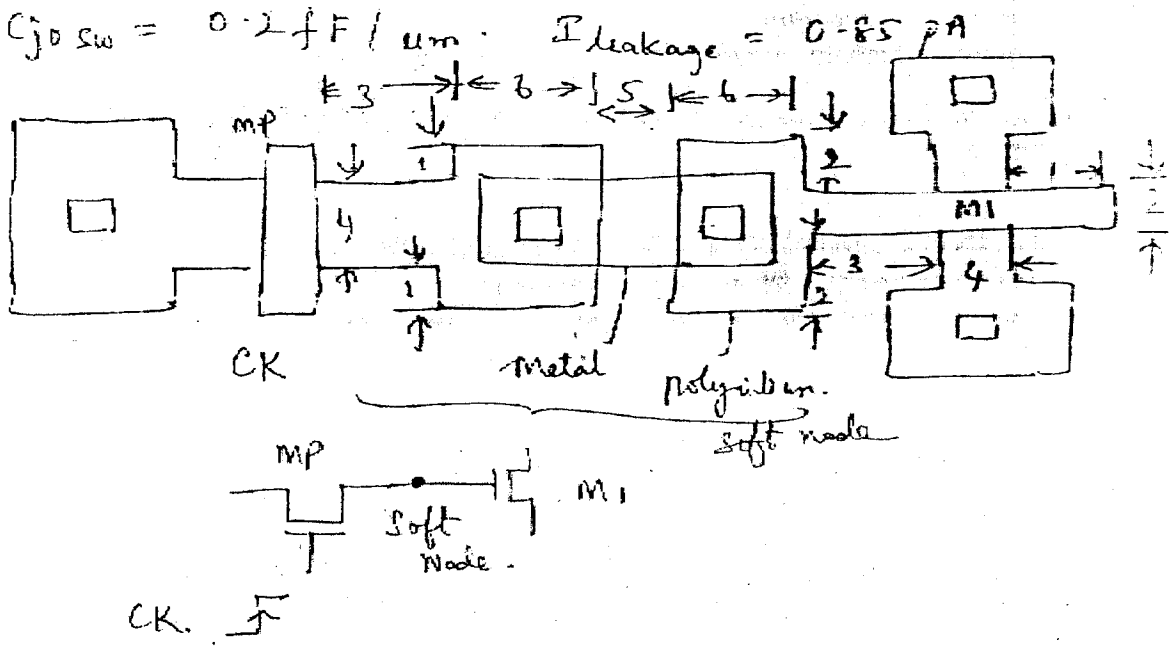

Fig. Q 5(c) (08 Marks)

6 a. Bring out the difference between Ratioed logic and ratio less logic with respect to 3 bit shift register. (06 Marks)

b. Dynamic CMOS logic circuit cannot be cascaded. Justify the statement. (06 Marks)

c. With relevant diagram, explain the NORA CMOS logi e[NP – Domino logid]. (08 Marks)

7 a. Explain with necessary expressions and transfer characteristics the differential amplifier. (08 Marks)

b. Discuss the general principle of the Band-gap reference and hence obtain expression for V_{BE}. (07 Marks)

c. Briefly explain the clock distribution network with relevant sketches. (05 Marks)

8 Write short notes on : (10 Marks)

a. Differential inverter

b. Complementary pass transistor logic (CPL)

c. Domino CMOS logic

d. Latch up phenomenon. (10 Marks)

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