USN | | | | | | | | | | |

10EC003

M.Tech. Degree Examination, December 2011
Advanced Computer Architecture

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions.***

1 a. With a diagram, explain the Flynn's classification of computer architectures. **(08 Marks)**

b. Compare i) UMA and NUMA models and ii) Implicit and Explicit parallelism. **(08 Marks)**

c. Determine the effective CPI and MIPs rate for the values in table Q.1(c), when clock frequency is 40MHz. **(04 Marks)**

Table Q.1(c)

Instn Type	Instn count	Clock cycle count
Integer arithmetic	45000	1
Data transfer	32000	2
Floating point	15000	3
Control transfer	5000	3

2 a. Differentiate between : i) Software and hardware parallelism ii) Control flow and demand driven computers. **(08 Marks)**

b. Describe program decomposition for static multiprocessor scheduling for a 2 × 2 matrix multiplication case. Assume suitable values and compare sequential and parallel scheduling for fine grain program graph. **(08 Marks)**

c. Explain i) control dependence and ii) Bernstein's conditions. **(04 Marks)**

3 a. Define Amdahl's law. Describe Amdahl's law for a fixed load, with equations and graphs. **(08 Marks)**

b. Explain i) Arithmetic mean performance ii) Harmonic mean speed up iii) System efficiency and iv) Quality of parallislism. **(08 Marks)**

c. If $O(1) = T(1) = n^3$, $O(n) = n^3 + n^2 \log_2 n$ and $T(n) = 4n^3/(n+3)$, determine speedup and efficiency when n = 16. **(04 Marks)**

4 a. Describe the architectural features of IBM RS/6000, a superscalar RISC processor. **(08 Marks)**

b. With a block diagram and a timing diagram, describe VLIW processor architecture. **(08 Marks)**

c. Compare RISC and CISC architectures. **(04 Marks)**

5 a. How does an asynchronous pipeline differ from a synchronous linear pipeline? Determine the speedup and efficiency if 4000 instructions are executed in a linear 6 stage pipelined processor working at a clock frequency of 20 MHz. **(08 Marks)**

b. For the reservation table Q5(b), determine the initial collision vector, forbidden latencies, state transition diagram and MAL. **(08 Marks)**

Table Q5(b)

S_1	X			X
S_2		X		
S_3			X	

c. With a diagram, explain the use of prefetch buffers. **(04 Marks)**

6 a. Explain memory hierarchy and derive the equation for effective memory access time. **(08 Marks)**

b. Describe address translation mechanism using TLB in virtual memory organization. **(08 Marks)**

c. Define the terms paging, cache mins, cache coherence and inclusion property. **(04 Marks)**

7 a. With a diagram, describe MESI cache coherence protocol. How does it differ from MSI protocol? **(10 Marks)**

b. Describe directory based cache coherence protocol. **(10 Marks)**

8 a. Explain multithreaded computations, with a diagram. What are the two problems of asynchrony? **(10 Marks)**

b. With a diagram, describe dataflow graph and dataflow machine. What are the differences between static and dynamic dataflow? **(10 Marks)**

*****