

# CBCS SCHEME

USN

--	--	--	--	--	--	--	--	--	--

18EC72

Seventh Semester B.E. Degree Examination, June/July 2024

## VLSI Design

Time: 3 hrs.

Max. Marks: 100

*Note: Answer any FIVE full questions, choosing ONE full question from each module.*

### Module-1

- 1 a. Define Moore's law. (02 Marks)  
b. Consider the design of a CMOS compound OR-OR-AND invert gate computing  $F = (A + B) \cdot (C + D)$ .  
(i) Sketch a transistor level schematic  
(ii) Sketch a stick diagram  
(iii) Estimate area from a stick diagram. (10 Marks)  
c. Derive the transfer characteristics of CMOS Inverter (graphical). (08 Marks)

OR

- 2 a. Explain all the non-ideal effects in MOS transistor. (10 Marks)  
b. With neat sketches explain the operation of MOSFET and derive the equation for drain current in all the regions. (10 Marks)

### Module-2

- 3 a. Explain VLSI design flow. (10 Marks)  
b. What is scaling? What are types of scaling and write scaling factors for device parameters? (10 Marks)

OR

- 4 a. Draw the schematic and layout of two input NAND gate. (06 Marks)  
b. Explain layout design rules for well, transistor rule and metal rules. (08 Marks)  
c. Define terms: (i) Metallization (ii) Passivation (iii) Metrology (06 Marks)

### Module-3

- 5 a. Explain Elmore delay model. (03 Marks)  
b. Define logical effort. Write the logical efforts of common gates. (10 Marks)  
c. Estimate the delay of the Fanout - of - 4 (FO4) inverter shown in Fig.Q5(c). Assume the inverter is constructed in a 180 nm process with  $\tau = 15$  ps.

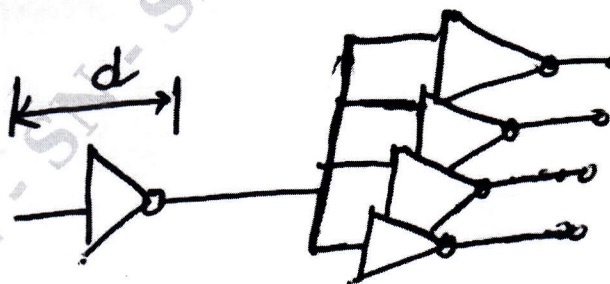


Fig.Q5(c)

(07 Marks)

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.  
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

OR

- 6 a. What is Ratioed logic? Explain following ratioed logic circuits:  
 (i) Pseudo nMOS  
 (ii) Ganged CMOS  
 (iii) Source follower pull-up logic (12 Marks)  
 b. Explain Cascade Voltage Switch Logic (CVSL). Realize the input AND/NAND using CVSL. (08 Marks)

**Module-4**

- 7 a. Explain the general structure of ratioed synchronous dynamic circuits. (05 Marks)  
 b. With necessary circuit diagram, explain dynamic shift register (ratioless) with enhancement load. (08 Marks)  
 c. What are the advantages of dynamic CMOS logic and explain the working of dynamic CMOS inverter. (07 Marks)

OR

- 8 a. Write the basic building block of a CMOS transmission gate dynamic shift register. (04 Marks)  
 b. With generalized circuit diagram, explain domino CMOS logic and using the same realize the following Boolean function:  $Z = AB + (C + D)(E + F) + GH$  (11 Marks)  
 c. With necessary diagram, explain a D flipflop with two phase non-overlapping clocks. (05 Marks)

**Module-5**

- 9 a. With neat circuit diagram, explain full CMOS SRAM cell. (08 Marks)  
 b. Draw the circuit of 3-bit BIST register and explain. (06 Marks)  
 c. Explain the terms: (i) Observability (ii) Fault coverage (iii) Controllability (06 Marks)

OR

- 10 a. With necessary circuit diagram, explain the operation of three transistor DRAM cell. (08 Marks)  
 b. What is a fault model? Explain stuck-at model with examples. (07 Marks)  
 c. Explain the logic verification principles. (05 Marks)

\*\*\*\*\*