CBCS SCHEME

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20ELD31

Third Semester M.Tech. Degree Examination, Jan./Feb. 2023
Synthesis Optimization of Digital Circuits

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. State and illustrate the different quality measures used in the optimization of the circuit used in the computer aided synthesis and optimization. **(10 Marks)**

b. Write a structural representation on verilog for a 5 bit ripple carry adder using 1 bit full adder. **(10 Marks)**

OR

2 a. Bring out the difference between different levels in the synthesis task used in computer aided synthesis and optimization. **(10 Marks)**

b. What are the different structural representations used in case of abstract models used to represent different circuit views at the logic and architectural levels which are based on the graphs. **(10 Marks)**

Module-2

3 a. For the function f = ab + bc + ac, find Boolean difference, consensus and smoothing with respect to 'a'. Represent the function and the above in the 3D Boolean space diagram. **(10 Marks)**

b. Comment on the components of the data path in the area estimation of the general circuits. **(10 Marks)**

OR

4 a. For shown in Fig.Q4(a), find the size of the maximum clique, clique cover number, largest stable set, stability number, minimum coloring and chromatic number. What is the condition for a graph is said to be perfect and graph is perfect?

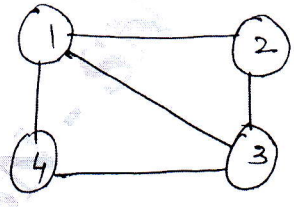

Fig.Q4(a) **(10 Marks)**

b. Show the scheduled sequencing graph under resource constraints for the graph show in Fig.Q4(b).

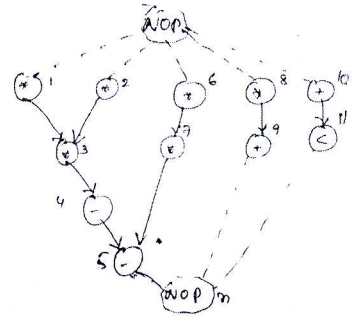

Fig. Q4(b) **(10 Marks)**

Module-3

5 a. For the function $f_1 = a'b' + b'c + ab$ and $f_2 = b'c$, show the Tabular representation and transistor–level schematic representation. **(10 Marks)**

b. Consider a networks with the following expression :

$f_x = ace + bce + de + g$

$f_y = ad + bd + cde + ge$

$f_z = abc$

Compute the Kervel set. **(10 Marks)**

OR

6 a. Consider three–input, two output function : $f = \begin{bmatrix} f_1 \\ f_2 \end{bmatrix}$

where $f_1 = a'b'c' + a'b'c + ab'c + abc + abc$ and $f_2 = a'b'c + ab'c$,

Find minimum cover, irredundant cover and minimal cover. Also represent the minimum cover in 3D Boolean space diagram. **(10 Marks)**

b. What are the different transformation used in logic networks and describe how they different form one another by giving the definitions of each. **(10 Marks)**

Module-4

7 a. Explain state Encoding problem for two level logic minimization. **(10 Marks)**

b. Explain the concept of implicit state minimization. **(10 Marks)**

OR

8 a. For the following set of equations, write, the synchronous circuit and synchrous logic network.

$a^{(n)} = i^{(n)} \bar{\oplus} i^{(n-1)}$; $b^{(n)} = i^{(n-1)} \bar{\oplus} i^{(n-2)}$;

$c^{(n)} = a^{(n)} b^{(n)}$; $d^{(n)} = c^{(n)} + d'^{(n-1)}$

$e^{(n)} = d^{(n)} e^{(n-1)} + d'^{(n)} b'^{(n)}$

$v^{(n)} = c^{(n)}$; $s^{(n)} = e^{(n-1)}$. **(10 Marks)**

b. Explain modeling and assumptions for retiming for the sequential network models. **(10 Marks)**

Module-5

9 a. For the data flow graph shown on Fig.Q9(a), write ASAP schedule diagram and ALAP schedule under latency constraints.

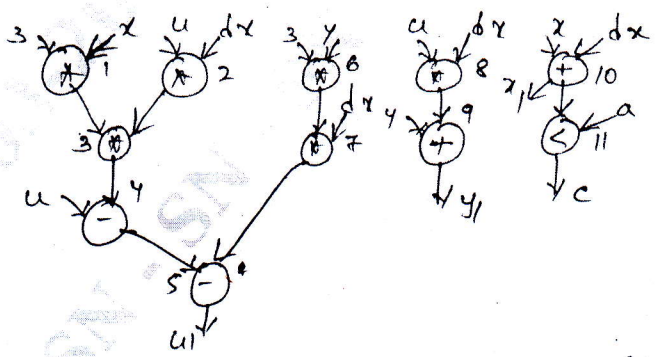

Fig.Q9(a) **(10 Marks)**

b. Explain sharing and binding for resource, dominated circuits. **(10 Marks)**

OR

10 a. Explain relative scheduling under timing constraints. **(10 Marks)**

b. Explain unconstrained minimum area binding for general circuits. **(10 Marks)**

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